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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/346,283	07/01/1999	MICHAEL R. FLANNERY	450.202US1	2222

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/346,283	FLANNERY, MICHAEL R.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 7, 12-18, 22, 25 and 26 are still rejected under 35 U.S.C. 102(b) as being anticipated by Kusunoki (US Pat. No. 5,324,980).

Regarding claims 1 and 12-15, Kusunoki teaches an integrated circuit with a micromechanical element comprising a semiconductor support substrate (901b) (see fig. 20F) supporting a micromechanical sensor element (916) (see fig. 20F), a logic circuit (915) (see fig. 20F) and a semiconductor visual display element (922) (see fig. 20F), the sensor element (916) electrically connected to the logic circuit (915) (see col. 25, lines 31-32), and the logic circuit (915) being electrically connected to the semiconductor visual display element (922) (see col. 25, lines 5-8).

Regarding claim 2, Kusunoki further teaches that said semiconductor display element (922) comprises an array of light-emitting pn junctions (see col. 25, lines 3-5).

Regarding claims 7 and 17, Kusunoki further teaches that said sensor element (916) is selected from the group consisting of strain gauges, thermal gauges, radiation gauges, and chemically responsive gauges (see col. 25, lines 28-31).

Regarding claim 16, Kusunoki further teaches wherein the input element (916) is selected from a group consisting of an inertial sensor and an accelerometer (see col. 25, lines 47-48).

Regarding claim 18, Kusunoki further teaches wherein the micromechanical sensor element (916) is configured to generate an electrical signal in response to an environmental or conditional change (see col. 25, lines 42-46).

Regarding claim 22, Kusunoki further teaches wherein the visual display element (922) provides a visual indication of a condition sensed by the sensor element (916) (see last two sentences of abstract).

Regarding claim 25, Kusunoki teaches an integrated circuit provided on a substrate with a unified input element and display element, the integrated circuit comprising: a moveable microengineered input element (916) supported by the substrate (901b) that senses a condition (see fig. 20F and last two sentences of abstract); a logic circuit (915) configured on the substrate and electrically connected to the input element (see fig. 20F and col. 25, lines 30-32); and a visual display element (922) supported by the substrate and coupled to the logic circuit (see fig. 20F and col. 25, lines 5-7) to provides a visual image; wherein the visual image is a visual representation of the sensed condition (see last two sentences of the abstract).

Regarding claim 26, Kusunoki teaches 26 an integrated circuit provided on a substrate with a unified input element and display element, the integrated circuit comprising: a moveable microengineered input element (916) supported by the substrate (901b) that senses a condition (see fig. 20F and last two sentences of

abstract), wherein the input element is a strain gauge (see col. 25, lines 47-48), a logic circuit (915) configured on the substrate and electrically connected to the input element (see fig. 20F and col. 25, lines 30-32); and a visual display element (922) having multiple light-emitting pn junctions supported by the substrate and coupled to the logic circuit (see fig. 20F and col. 25, lines 3-7), wherein the visual display element provides a visual image comprising a visual representation of the sensed condition (see last two sentences of the abstract).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-6, 19-21, 23 and 24 are still rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki (US Pat. No. 5,324,980) in view of Holm et al. (US Pat. No. 5,501,990).

Regarding claims 3-6 and 19, Kusunoki fail to teach that said visual display comprises an of GaAs light-emitting pn junctions and/or an array of semiconductor pixels having a pitch of about 20 μm. Holm et al. teaches that it is well known in the art to use GaAs LEDs having a pixel pitch dimension of less than 20 μm as display devices (see col. 1, lines 15-17 and 20-22, col. 3, lines 25-60, and col. 6, lines 1-2).

Kusunoki and Holm et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a visual display element comprising GaAs LEDs having a pixel pitch of less than 20 μm. The motivation for doing so, as is taught by Holm et al., is to provide a high quality image (col. 5, lines 39-42). Therefore, it would have been obvious to combine Holm et al. with Kusunoki to obtain the invention of claims 3-6, 19-21, 23 and 24.

Regarding claims 20, 23 and 24, Holm et al. further teaches that it is well known in the art that an array of LEDs is used to form complete images containing pictorial (e.g. colors) and/or alphanumeric characters (see col. 1, lines 20-22).

Regarding claim 21, Kusunoki further teaches wherein the input element is a first input element, the integrated circuit further comprising: a second input element (see col. 27, lines 52-56, wherein Kusunoki teaches the limitation of providing a plurality of sensor elements in the single chip).

Response to Arguments

5. Applicant's arguments filed October 29, 2004 have been fully considered but they are not persuasive. Applicant argues that the prior art does not teach "a semiconductor support substrate." However, this argument is not persuasive. The court has held that during patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification. *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). In the instance case, the broadest reasonable

interpretation for the term "a semiconductor support substrate" is any substrate supporting a semiconductor structure. Kusunoki, as stated before, does teach the limitation in figure 20F by showing substrate (901b) supporting a semiconductor structure (consider layers 922, 915, 902, and 916). Therefore, the rejection is considered to be proper.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Zhang et al. (US Pat. No. 6,274,861 B1) teaches a sensor (30), a display (20) and a logic circuit (40) integrated on a single substrate (10) (see fig. 1).

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
1/9/05

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